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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/644,225	08/19/2003	Igor Keller	02PA053US01	6463

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EXAMINER	
PIERRE LOUIS, ANDRE	

ART UNIT	PAPER NUMBER
2123	

MAIL DATE	DELIVERY MODE
11/24/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)
	10/644,225	KELLER, IGOR
	Examiner	Art Unit
	ANDRE PIERRE LOUIS	2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 September 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 9/13/2010 has been received and fully considered.

2. Claims 1-41 remain pending and are presented for examination.

Response to Arguments

3. Applicant's arguments filed 9/13/2010 have been fully considered but they are not persuasive.

3.1 Applicant argues the cited does teach the selecting step of the claims, the Examiner respectfully notes that Lee does disclose the selection of latest signals with the latest arrival to represent the worst case timing event *(see col.1 lines 23-27, col.4 lines 9-43, col.7 lines 27-31, just to name a few)*, wherein a plurality of timing events are propagated from the primary inputs to through the input of the gates *(see further col.15 line 44-col.16 line 56)* and would clearly be understood by one of ordinary skilled in the art. Yalcin et al., used as a secondary reference in the rejection, substantially teaches a timing analysis, including the selection of a plurality of timing events, such as "fast" and "slow" slew inputs and capacitive loading to generate a model based said input timing events *(para 55-56, 60-63, 114)*. The Examiner further notes that while a small portion of the prior were cited in the rejection, the references should be considered entirely by the applicant.

3.2 While the applicant believes that the independent claims, along with the dependent claims should be found allowable, the examiner respectfully disagrees and asserts that the combined references cited teach the entire claimed invention. *Applicant is further encouraged to look at the additional references cited but not used shown in the conclusion*

section of this and/or the previous office. However, the grounds of rejections below fully support the Examiner's position in rejecting the instant claims.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4.0 Claims 1-41 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Lee ET al. (U.S. Patent No. 6,430,731), in view of Yalcin et al. (USPG_PUB No. 2003/0140324).

4.1 In considering the independent claims 1,6, 11, 19, 29, and 33, Lee et al. substantially teaches a computer implemented method for determining a worst-case transition, and particularly teaches the steps of: determining a first output timing event at an output of a gate for a first input timing event at an input of the gate based at least in part upon a timing model of the gate *(col.2 lines 16-33 and col.7 lines 4-30)*; determining a second output timing event at the output of a gate for a second input timing event at the input of the gate based at least in part upon the timing model of the gate *(col.2 lines 16-33 and col.7 lines 4-30);* selecting, by using a processor, the first input timing event corresponding to the first output timing event as a worst case timing event if the first output timing event has a later arrival time of transitions at the output of the gate than the second output timing event and selecting the second input timing event corresponding to the second output timing event as a worst case timing event if the second output timing event has a later arrival time of transitions at the output of the gate than the first output timing event, such that the one of a plurality of timing events propagated to the input of

the gate with a worst output slew or output delay as a function of input slew at the output of the gate is selected as the worst case timing event *(fig.11, col.1 lines 23-27, col.4 lines 27-43, and col.6 line 31- col.7 line 31, and col.15 lines 42-col.16 line 42);* storing information related to the worst case timing event in a computer readable medium *(col.14 lines 40-43 and col.15 lines 52-62).* While Lee equation does not clearly show that his load data loading is part of his calculation, as shown in *claims 19 and 33*, he discloses taking into consideration parameters such as the capacitive loading of the model *(see col.4 lines 37-49)*, and *col.5 line 1-15* shows a detailed spice simulation for static CMOS gates under different slew and capacitance loading conditions, and would clearly be understood be one of skilled in the art. Lee further teaches the processor and readable medium of claim 6 *(see fig.12 (210-220));* the step of identifying the plurality of timing events propagated to an input of the gate having different arrival time at an input of the gate (*(fig.11, col.2 lines 21-33, col.4 lines 9-43, col.15 lines 42-col.16 line 42*); determining the different slews from the plurality of timing events, shown also in *claim 29 and 33* (see *(fig.11, col.4 lines 9-43, col.7 lines 4- 31, and col.15 lines 42-col.16 line 42);* processor and readable medium of *claim 6 (see fig.12 (210-220)).* Nevertheless, Yalcin et al. substantially teaches generating a TLF model based upon inputs slew and capacitance loading selected *(para 55-56, 60-63, 114).* Lee and Yalcin are analogous art because they are from the same field of endeavor and that the model analyzes by Yalcin is similar to that of Lee. Therefore, it would have been obvious to one of ordinary skilled in the art to combine the ing analysis of Yalcin with the method and apparatus of Lee because Yalcin teaches the advantage of speeding up timing analysis *(see para 85).*

4.2 As per claims 2,7, 12, and 20, the combined teachings of Lee et al. Yalcin substantially teach the step of determining a plurality of gate delays for a plurality of input signals based at least in part upon the timing model of the gate *(see Lee et al. col.4 lines 27-43; also see Yalcin para 55, 63, 114*).

4.3 With regards to claims 3,8, 13, and 21, the combined teachings of Lee et al. Yalcin substantially teach that the step of selecting the worst-case input timing event further comprises the step of selecting a worst delay based at least in part upon the gate delays *(see Lee et al. col.15 lines 44-48).*

4.4 Regarding claims 4,9, 14, and 22, the combined teachings of Lee et al. Yalcin substantially teach that the timing model comprises $To = Ti + Dg$, $Dg = F(S_1, C)$, $So = Q(S_1, C)$, where *To* is an output time, T_i is an input time, Dg is a gate delay, S_1 is an input slew, C is a capacitive load of the gate, and *So* is an output slew, wherein the delay *Dg* of the gate depends, at least in part , on the slew of the input transition and capacitive load at the output of the gate (*see Lee et al. col.4 lines 27-43, also see Yalcin para 55-56, 60-63, 114).*

4.5 Regarding claims 5,10, 15, and 23, the combined teachings of Lee et al. Yalcin substantially teach that the timing model is a timing library format (FTL) model (*see Lee et al. col.5 lines 7-17, also see Yalcin para 59-63*).

4.6 With regards to claims 16-18, the combined teachings of Lee et al. Yalcin substantially teach that the output slews of the output timing events includes slew rate of the output timings, which is determined by an amount of time for a waveform to transition from a first voltage to a second voltage *(see Lee et al. col.2 lines 16-33).*

4.7 Regarding claim 24, the combined teachings of Lee et al. Yalcin substantially teach that the different arrival times comprise the arrival times of the timing event at each input of the gate *(see Lee et al. col.2 lines 16-33 and col.4 lines 9-43)*.

4.8 As per claim 25, the combined teachings of Lee et al. Yalcin substantially teach that the different arrival times of the timing event at each input of the gate comprises the input times of the timing events *(see Lee et al. col.2 lines 16-33 and col.4 lines 9-43)*.

4.9 With regards to claims 26,30, and 34, the combined teachings of Lee et al. Yalcin substantially teach that the different slews comprise transition times of the timing events through the gate *(see Lee et al. col.3 line 65-col.4 lines 43)*.

4.10 Regarding claims 27,31, and 35, the combined teachings of Lee et al. Yalcin substantially teach that the transition times of the timing events through the gate are based at least in part upon characteristics of the gate *(see Lee et al. col.3 line 65-col.4 lines 43, also Yalcin para 65, 114)*.

4.11 As per claims 28,32, and 36, the combined teachings of Lee et al. Yalcin substantially teach that a duration of the transition times of the timing events through the gate is based at least in part upon characteristics of the gate *(see Lee et al. col.3 line 65-col.4 lines 43)*.

4.12 With regards to claims 37-41, the combined teachings of Lee et al. Yalcin substantially teach that information related to the worst-case timing event is stored in a memory *(see Lee et al. col.14 lines 40-43 and col.15 lines 52-62)*.

Conclusion

5. Claims 1-41 are rejected and **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andre Pierre-Louis whose telephone number is 571-272-8636. The examiner can normally be reached on Mon-Fri, 8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul L. Rodriguez can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/A. P. L./
Examiner, Art Unit 2123
November 20, 2010

/Paul L Rodriguez/

Supervisory Patent Examiner, Art Unit 2123